BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

REMARKS

At the time of the Office Action dated December 17, 2003, claims 1-5 and 12-20 were pending in this application. Of those claims, claims 1-5 have been rejected and claims 12-20 have been withdrawn from consideration pursuant to the provisions of 37 C.F.R. § 1.142(b).

On page two of the Office Action, the Examiner objected to the drawings pursuant to 37 C.F.R. § 1.83(a), requiring depiction of the claimed conductive parts on the chip in claims 1 and 2. In response, it is proposed to amend Figs. 7A and 7B to depict multiple bonding pads. As bonding pads are conductive, these bonding pads can illustrate the claimed conductive parts. Applicant, therefore, respectfully submits that the imposed objection to the drawings has been overcome and, hence, solicit withdrawal thereof.

CLAIM 4 IS REJECTED UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY SHIGENO ET AL., U.S. PATENT NO. 6,372,625 (HEREINAFTER SHIGENO)

On pages three and four of the Office Action, the Examiner asserted that Shigeno discloses a semiconductor device corresponding to that claimed. This rejection is respectfully traversed.

In the Amendment filed October 1, 2003, Applicant traversed the Examiner's prior rejection of claim 4 for anticipation based upon Shigeno on several grounds. However, in the present Office Action, in the section entitled "Response to Arguments," the Examiner responded to only one of these grounds. In this regard, the Examiner is referred to M.P.E.P. § 707.07(f),

which states that "the Examiner, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it."

Claim 4 recites, in part, the following limitations: "each of said bonding wires has a plurality of bends ... at least one of said plurality of bends is exposed on a surface of said sealing resin package." As to this particular limitation, the Examiner referred to the dotted line[1] in Fig. 2 of Shigeno. *Assuming arguendo* that the dotted line represents an actual feature in the structure illustrated by Fig. 2, the wire represented by dotted line does not meet the limitations recited in claim 4 because the dotted line wire does not have a plurality of bends. Applicant notes that this was one of the arguments presented in the Amendment filed October 1, 2003, that was not responded to by the Examiner.

A question that the Examiner has apparently not considered is: why is the wire in Fig. 2 referred to by the Examiner represented by dotted lines instead of solid lines? The answer to this question explains why Shigeno does not teach that the dotted line includes an exposed bend. According to Shigeno, Fig. 2 illustrates "an embodiment of the present invention" (column 3, lines 19-20). Shigeno also states that "[a] conventional bonding wire is shown by the dotted lines in FIG. 2" (column 4, lines 62-63). Thus, Shigeno distinguishes all the other features in Fig. 2 from the wire shown by dotted lines by explaining that the wire shown by dotted lines is a conventional bonding wire. Furthermore, the purpose of showing the conventional bonding wire in Fig. 2 is to compare wire 16 in Fig. 2 with the conventional wire. In particular, the comparison is to show how, in contrast to a conventional wire, a loop height t and a distance 50 from a chip end

[1] Although the Examiner referred to this feature with reference numeral 23, reference numeral 23 in Shigeno does not refer to the dotted line but instead refers to a bend in the wire (column 4, lines 36-37).

26 to a lead terminal 26 can be reduced by using wire 16 (column 4, line 67 – column 5, line 10). Thus, there is no indication in Shigeno that the conventional wire shown by dotted lines in Fig. 2 is intended to be associated with the other features in Fig. 2 except for comparison purposes.

The Examiner is also referred to Fig. 1 of Shigeno, which discloses a "conventional semiconductor device." Fig. 1 is used by Shigeno for contrasting with the semiconductor device disclosed by Fig. 2, and it is from Fig. 1 that the conventional wire shown by dotted lines is originally derived. As shown in Fig. 1 the bend B in wire 5 (which directly corresponds to the wire shown by dotted lines in Fig. 2) is well below the surface of the sealing resin package. Applicant also refers the Examiner to column 5, lines 7-11 of Shigeno, which describes that the reduction in height t realized by using the wire 16 in Fig. 2 allows for "the thickness of the molded resin body 17 [to be] reduced." Thus, *assuming arguendo* that the height of the molded resin body 17 package in Fig. 2 is lower the height of the wire shown by dotted lines, such an assumption is not germane to the claimed limitations. The relationship between the bend in the conventional wire shown by dotted lines in Fig. 2 and the surface of the resin body 6 is shown in Fig. 1 and the relationship between the bend 23 of the wire 16 and the surface of the resin body 17 is shown in Fig. 2, and <u>both</u> of Figs. 1 and 2 disclose that the bends (i.e., B and 23) are <u>below</u> the surfaces of the respective resin bodies 6, 17. Therefore, both Figs. 1 and 2 of Shigeno fail to disclose that "at least one of said plurality of bends is exposed on a surface of said sealing resin," as recited in claim 4.

The above argued differences between the claimed semiconductor device and the device of Shigeno undermine the factual determination that Shigeno identically describes the claimed invention within the meaning of 35 U.S.C. § 102. Applicant, therefore, respectfully submits that the

imposed rejection of claim 4 under 35 U.S.C. § 102 for anticipation based upon Shigeno is not factually viable and, hence, solicits withdrawal thereof.

CLAIMS 1, 2 AND 5 ARE REJECTED UNDER 35 U.S.C. § 103 FOR OBVIOUSNESS BASED UPON SHIGENO IN VIEW OF KUMAZAWA ET AL., U.S. PATENT NO. 5,156,323 (HEREINAFTER KUMAZAWA)

On pages five and six of the Office Action, the Examiner concluded that one having ordinary skill in the art would have been motivated to modify the semiconductor device of Shigeno in view of Kumazawa to arrive at the claimed invention. This rejection is respectfully traversed.

In the Amendment filed October 1, 2003, Applicant traversed the Examiner's prior rejection of claim 1[2] for obviousness based upon Shigeno in view of Kumazawa. In particular, Applicant argued that that one having ordinary skill in the art would not have been motivated to modify Shigeno in view of Kumazawa to arrive at the claimed invention since the Examiner had not established that the asserted benefits (i.e., "provide a protection against edge shorting and an increased wire loop length") are a result of the proposed modification (i.e., the nearest bend to the inner lead is at a level higher than that of the nearest bend to the chip).

As discussed above, M.P.E.P. § 707.07(f) states that "the Examiner, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it." In responding to Applicant's argument, the Examiner stated on page 8 of the Office Action the following:

[2] Claim 1 was previously amended to include the limitations of claim 6, which was the subject of the Examiner's prior rejection.

> A. Applicant contends that Kumazawa et al. do not teach in Fig. 3, the bend nearest to a bonding point on a work piece/lead frame substrate not being at a higher level than the bend nearest to bonding point on chip.
>
> However, as explained above, Kumazawa et al. teach in Fig. 4, the bend (1b in Fig. 4) nearest to a bonding point on a work piece/substrate (I in Fig. 4) being at a higher level than the bend (1a in Fig. 4) nearest to bonding point on chip (A on chip 3 in Fig. 4) to provide protection against edge shorting and an increased wire loop length (Col. 4, line 1-25).

In comparison, in the paragraph spanning pages 5 and 6 of the present Office Action, the Examiner stated:

> Kumazawa et al. teach using bonding wires having a plurality of bends such that the bend (1b in Fig. 4) nearest to a bonding point on a work piece/substrate (I in Fig. 4) is at a higher level than the bend (1 a in Fig. 4) nearest to bonding point on chip (A on chip 3 in Fig. 4) to provide a protection against edge shorting and an increased wire loop length (Col. 4, line 1-25).

In further comparison, the Examiner's original rejection on page 7 of the Office Action dated April 27, 2003, included the statement that:

> Kumazawa et al. teach using bonding wires having a plurality of bends such that the bend (1 a in Fig. 4) nearest to a bonding point on chip (A on chip 3 in Fig. 4) is at a higher level than the bend (1b in Fig. 4) nearest to a bonding point on a work piece/substrate (I in Fig. 4) to provide a protection against edge shorting and an increased wire loop length (Col. 4, line 1-25).

As evident from these passages, the Examiner statement of rejection in the present Office Action is nearly identical to the statement of rejection in the original Office Action except that the Examiner corrected a minor error involving the transposing of features. Also, the Examiner's "Response to Arguments" is nothing more than a word-for-word restatement of the rejection, which is nearly word-for-word identical to the original rejection. Thus, the Examiner has failed to put forth any substantive response to Applicant's arguments.

As argued in the Amendment filed October 1, 2003, there is no nexus between the proposed modification and the alleged benefit of preventing edge shorting and increasing a length of a wire loop. Kumazawa states that the benefit of preventing edge shorting and

increasing length of the wire loop is a result of the methodology disclosed by Kumazawa (column 4, lines 10-23) and not the structure of the wire bonds.

Applicant's reference to Fig. 3 in the Amendment filed October 1, 2003, is to illustrate what Kumazawa teaches to be the basis for the asserted benefits of providing protection against edge shorting and an increased wire loop. Both Figs. 3 and 4 are described as illustrating a wire loop" shaped by the method of the present invention" (column 2, lines 9-12) (emphasis added). Furthermore, Fig. 3 shows that a nearest bend (1b) to an inner lead is not at a level higher than that of a nearest bend (1a) to a chip. As Fig. 3 is disclosed as being an embodiment of the claimed invention, it stands to reason that having the nearest bend to the inner lead be at a level higher than that of the nearest bend to the chip is not a necessary requirement to obtain the asserted benefits of preventing edge shorting and increasing a length of a wire loop.

Therefore, one having ordinary skill in the art would not have been motivated to modify Shigeno in view of Kumazawa to arrive at the claimed invention to obtain the benefits of preventing edge shorting and increasing a length of a wire loop, because these benefits are not taught as being derived from the proposed modification. Applicant, therefore, respectfully solicits withdrawal of the imposed rejection of claims 1-2 and 5 under 35 U.S.C. § 103 for obviousness based upon Shigeno in view of Kumazawa.

CLAIM 3 IS REJECTED UNDER 35 U.S.C. § 103 FOR OBVIOUSNESS BASED UPON SHIGENO IN VIEW OF KUMAZAWA AND WARK ET AL., U.S. PATENT NO. 5,847,445 (HEREINAFTER WARK)

On page seven of the Office Action, the Examiner concluded that one having ordinary skill in the art would have been motivated to modify the semiconductor device of Shigeno in view of Kumazawa and Wark to arrive at the claimed invention. This rejection is respectfully traversed.

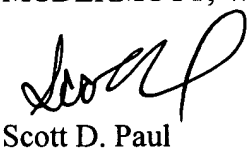
Claim 3 depends ultimately from independent claim 1, and Applicant incorporates therein the arguments previously advanced in traversing the imposed rejection of claim 1 under 35 U.S.C. § 103 for obviousness based upon Shigeno in view of Kumazawa. Specifically, one having ordinary skill in the art would not have been motivated to modify Shigeno in view of Kumazawa to arrive at the claimed invention. The tertiary reference to Wark does not cure the argued deficiencies of Shigeno and Kumazawa. Accordingly, the proposed combination of references would not yield the claimed invention. Applicant, therefore, respectfully submits that the imposed rejection of claim 3 under 35 U.S.C. § 103 for obviousness based upon Shigeno in view of Kumazawa and Wark is not viable and, hence, solicits withdrawal thereof.

Applicant has made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicant invites the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing remarks, Applicant hereby respectfully requests reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Scott D. Paul
Registration No. 42,984

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SDP/AJS:kap
Date: March 15, 2004
Facsimile: (202) 756-8087